REMARKS/ARGUMENTS

The Applicant calls attention to U.S. Patent Application Serial Number 10/759,583 filed January 15, 2004 in the name of the present inventor entitled Method and Apparatus for Image Processing. Such application, which is directed to a combination of an element for object-independent processing and an element for object-dependent processing is believed to have been approved by the Examiner for allowance over art of record in the present application. The present application claims further limitations over the combination of elements or layers for object- independent and object-dependent processing, namely, a third processing layer operative in real time to perform object recognition and association employing the dynamic feature set yielded by the second processing layer against an object to be recognized.

In specific reference to the present application, claims 1-9 and 11-18 stand rejected under 35 U.S.C. §103(a) as being obvious over Juvinall et al. in view of a paper by Chin et al. (both cited in the Information Disclosure Statement).

Claim 10 stands rejected under 35 U.S.C. §102(b) as being anticipated by the paper by Chin et al. (cited in the Information Disclosure Statement).

The Applicant respectfully traverses these rejections for the following reasons.

The subject matter of Juvinall, which was specifically cited by the Applicant, is the type of prior art with deficiencies that the present invention addresses to overcome. None of the art of record discloses computational structures or processing on a real-time basis to obtain a dynamic feature set for object recognition. None of the art of record discloses computational structures for performing, in real time, object recognition and association in a first, second and third processing layer employing that dynamic feature set against an object to be recognized.

For the type of computation contemplated, Juvinall is structurally insufficient, since it requires access to external memory, and is therefore subject to an significant input/output bottleneck. As to claims 2, 12 and 16, for example, Juvinall simply does not employ symmetric multi-processing.

In Chin, even though asserted otherwise, the second layer does not operate properly if implemented as an MPP SIMD. In fact, it will operate as a uniprocessor system,

since it would be necessary for the memory controller to serialize the parallel accesses to DRAM from the MPP SIMD itself. As evidence of this type of contention towards DRAM through a single, centralized DRAM controller, reference is made to the arguments by AMD against Intel-type processors with regard to sustainable performance versus peak performance obtained by using only data and instructions already present in their respective caches. The AMD argument is based on the fact that the relevant Intel architecture combines many CPU cores and connects them to a single set of DRAM controllers in an external MCH (Memory Control Hub) and therefore generates DRAM contention, whereas within the comparable AMD architecture, there is one set of DRAM controllers per processor die. The published literature identifies this as a problem with the structures and methodologies of the type described in the Chin reference. For example, reference is made to Digital Technical Journal Vol. 6, No. 2 a Cray Research Paper dated after April 1994 entitled "A Shared Memory MPP from Cray Research" by Koeninger, Furtney and Walker, a copy of which is attached hereto. This document indicates that the problem has long been known and to the date of this filing had still not been solved. Further reference is made to a white paper dated by AMD on July 15, 2003 entitled "AMD Operon™ Processor Benchmarking for Clustered Systems," by O'Flaherty and Goddard. This attached paper discusses the bottleneck issue and compares AMD and Intel processing unit architectures. These documents show that, even after many years of knowledge of this issue, problems persisted, and nothing suggested solutions of the type herein claimed.

The present invention employs a second layer for object-dependent processing. In more specific articulation (e.g., claims 2 and 12), the second layer for object-dependent processing is a true SMP (symmetric multi-processor), making it even more clear that it is not an MPP SIMD. To emphasize these distinctions, the dependency of claims 11 and 12 have been changed.

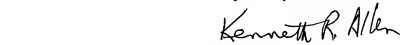
Therefore, the Applicant submits that the claimed subject matter clearly distinguishes over the art of record, either alone or in combination, and is therefore not obvious to those of ordinary skill in the art and thereby defines patentable subject matter.

CONCLUSION

In view of the foregoing, the Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 326-2400.

Respectfully submitted,



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